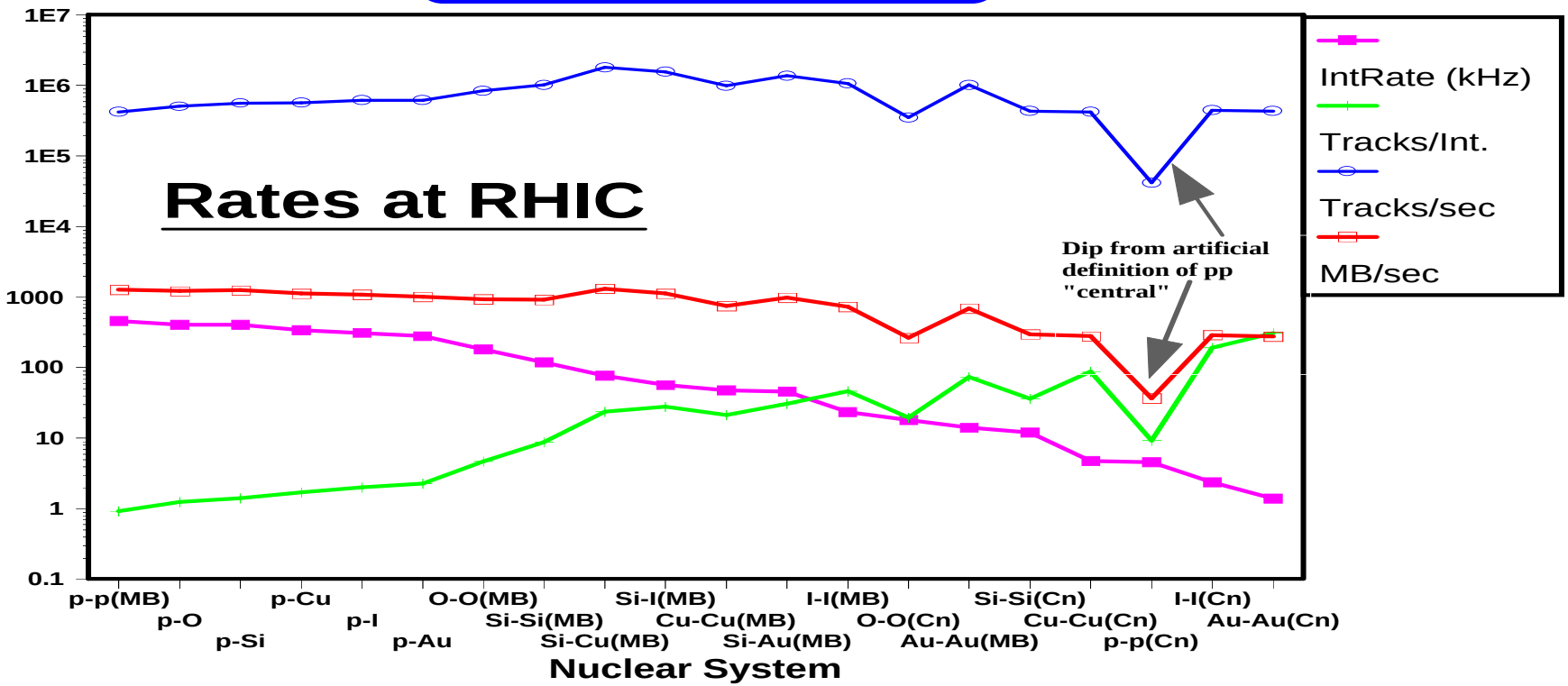
PHENIX Readout system

- What RHIC, PHENIX demand….
- General system parameters
- FEM (front-end Modules)
- GTM (granule timing module)
- Level 1 Trigger (skip..)
- DCM (data collection module)
- EVB (event Builder) (skip…)
- Upgrade works

PHENIX DAQ


Rates at RHIC
1E7
1E6
1E5
1E4
1000
100
10
1
0.1
IntRate (kHz)
Tracks/Int.
Tracks/sec
MB/sec
Dip from artificial definition of pp "central"
p-p(MB)
p-O
p-Si
p-Cu
p-I
p-Au
O-O(MB)
Si-Si(MB)
Si-Cu(MB)
Si-I(MB)
Cu-Cu(MB)
Si-Au(MB)
I-I(MB)
O-O(Cn)
Au-Au(MB)
Si-Si(Cn)
Cu-Cu(Cn)
p-p(Cn)
I-I(Cn)
Au-Au(Cn)
Nuclear System

System overview

- **~ 300,000 channels**
- Front end electronics close or on the detector
- Beam Crossing clock = **106 ns**
- Level-1 trigger latency 40 beam crossing clocks
- Maximum Average Level-1 trigger rate **25 kHz (12.5KHz)**
  - Most likely will change to 20KHz for the silicon detector
- **Fully pipelined**, **simultaneous Read/Write**
- 5 Level-1 accepted event buffer at Front-end Module
- Front End Electronics send uncompressed data to Data Collection Modules (fix format and timing)
- Detector occupancy ranges from
  - p + p (a few tracks) to Au + Au (2.5 - 10%)

PHENIX ONLINE SYSTEM

Fully pipelined system

Max. L1 trigger rate **25** (12.5) KHz

L1 Delay 40 beam clock

9.8 MHz beam clock

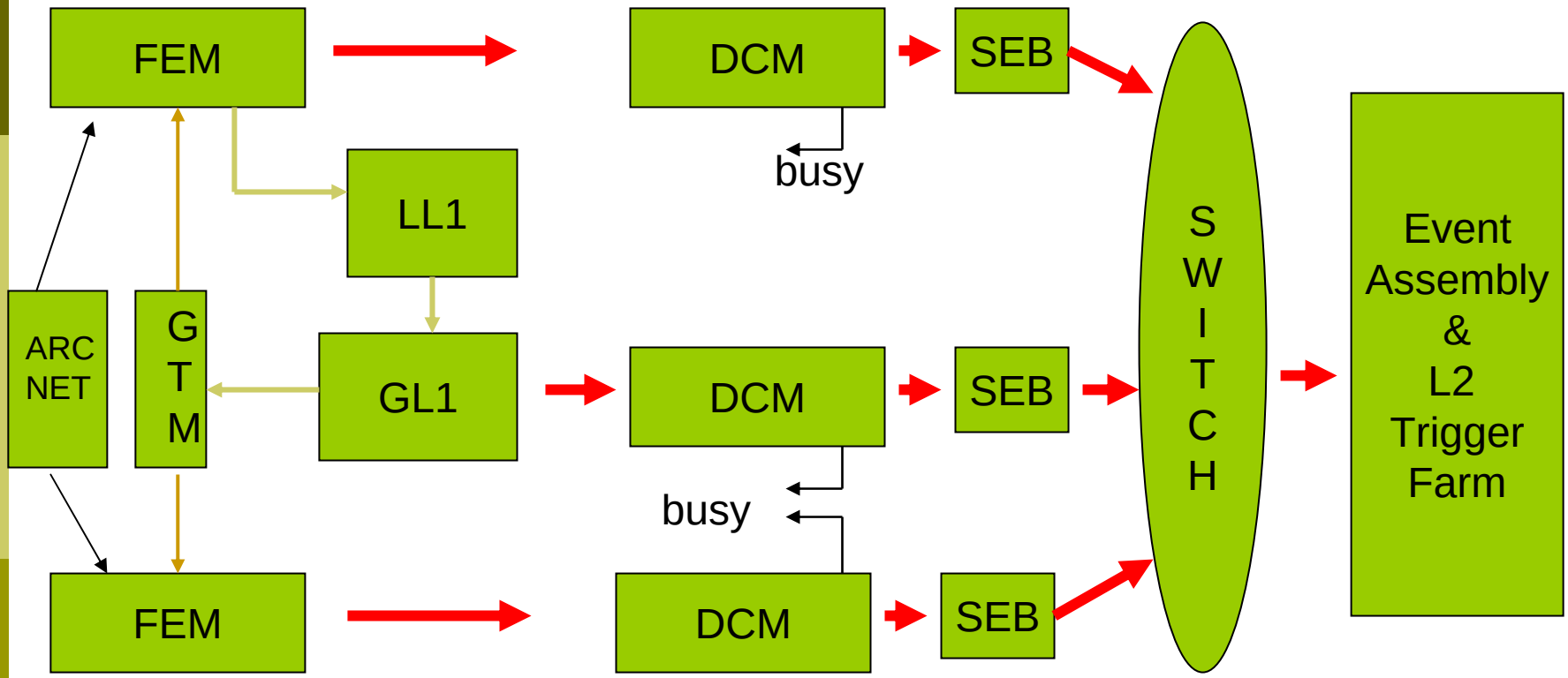
FEM: FrontEnd Module

DCM: Data Collection Module

GTM: Granule Timing Module

L1 : Level 1 Trigger

SEB: Sub-event Buffer



FEM can hold up to 5 L1 accept events

Data transfer to DCM via gigabit optical fiber

Zero suppression is performed by DCM

A few points on the PHENIX Online System

- Horizontal Integration
  - Long argument before design is final
  - Integration is smooth.
  - Easier to add new detectors.
- Small groups
  - FEM
    - ORNL, Columbia University, LANL, BNL, Stony Brook, LLNL, U. Tokyo, Lund
  - Level 1
    - Iowa State
  - Timing System
    - BNL
  - DCM
    - Columbia University, Colorado
  - Event Builder
    - Columbia University, BNL, Georgia State

PHENIX Online System

FEM:

- **Record detector signals.**
- **Buffer data for 40 beam crossing. (L1 delay)**
- **Simultaneous read/write.**
- **Provide 5 triggered event buffers.**
- **send un-zero suppression data. – No busy**

GTM:

Provide Clock, L1 trigger and L0 timing information to FEM.

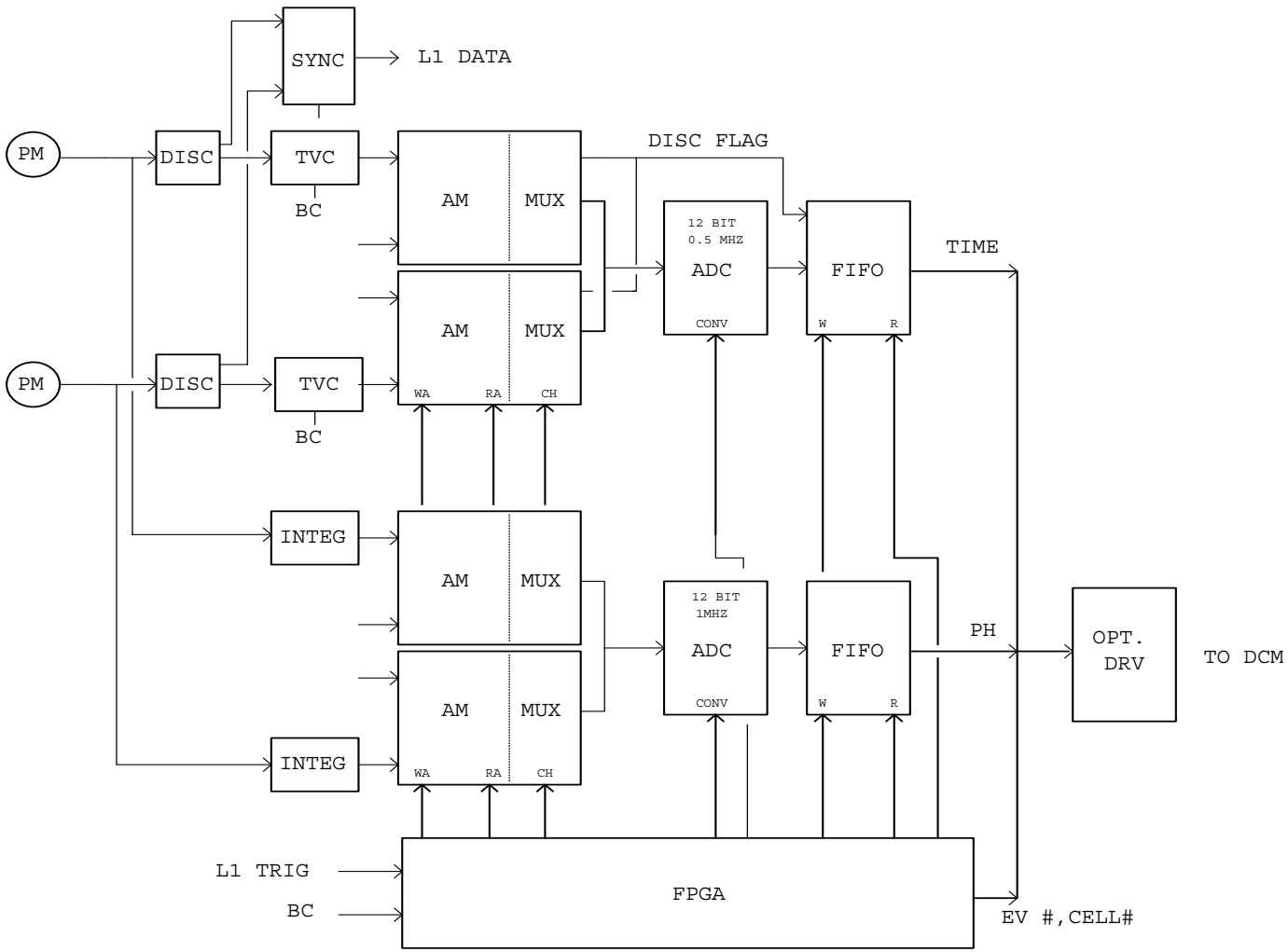
L1 Trigger:

- **Receive trigger primitives.**
- **Generate L1 trigger.**
- **Facilitate partition running mode .**

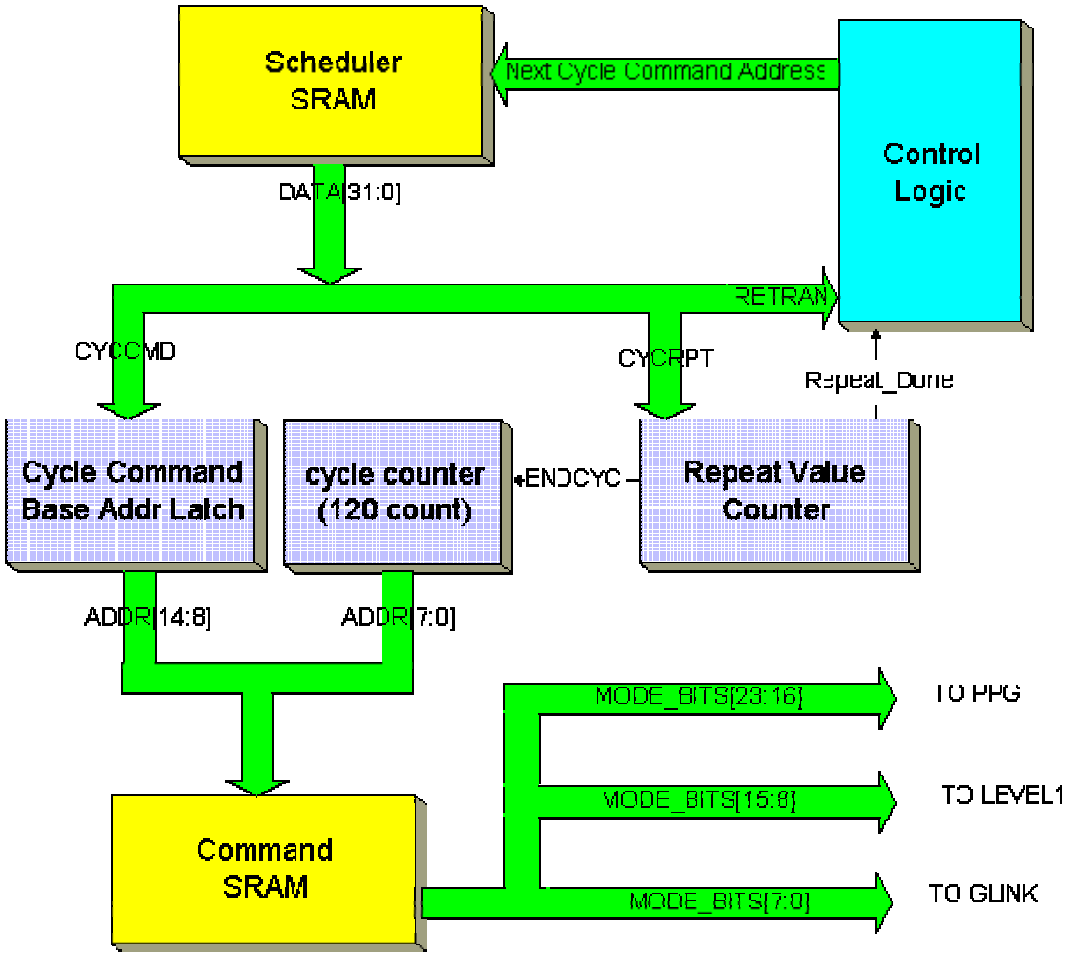
DCM:

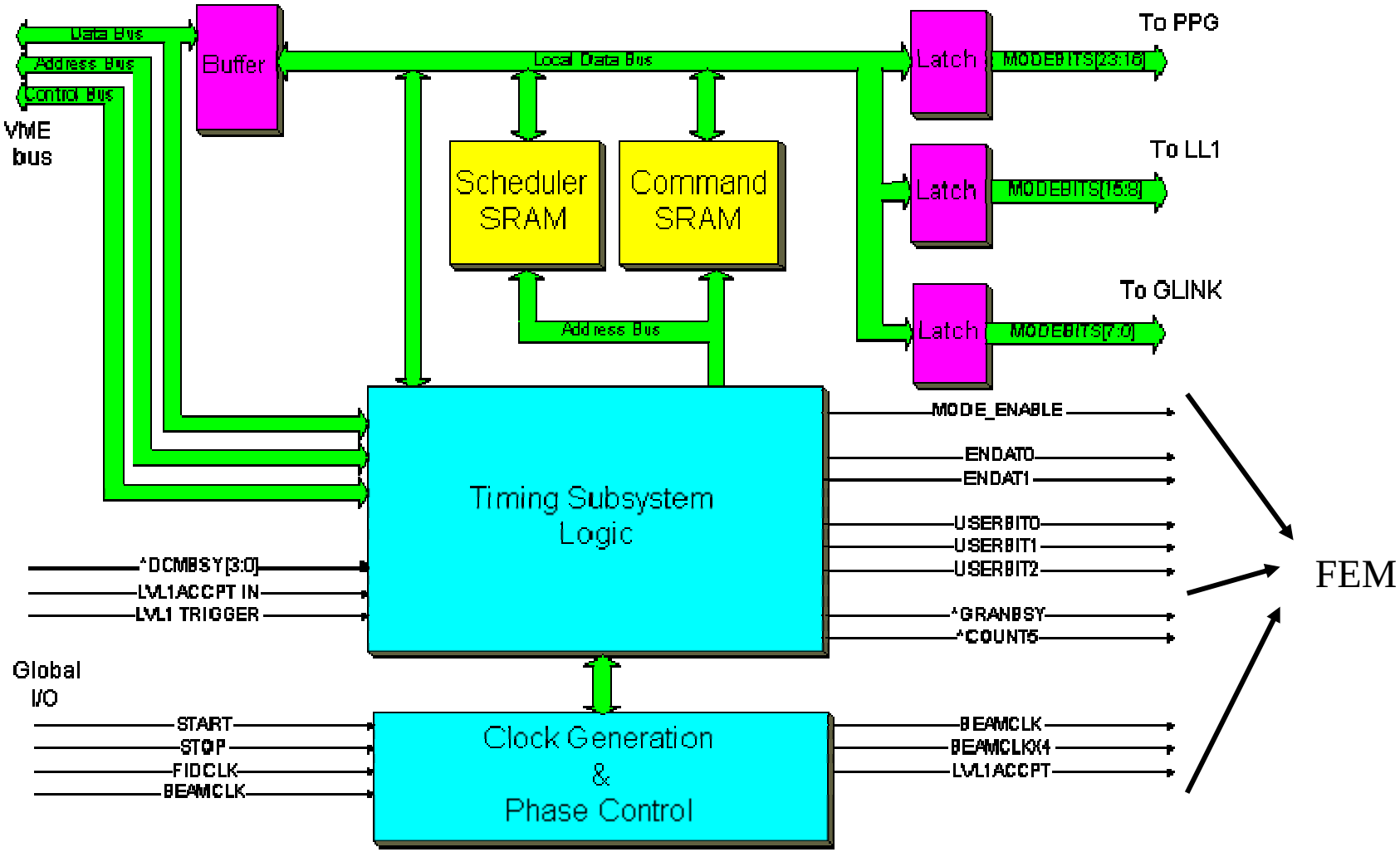
- **Receive FEM data, zero suppression FEM data, check data integrity.**
- **Provide 5 event buffers as well as many zero suppressed event buffers.**
- **First stage of the event building.**
- **Generate L2 trigger primitives.**
- **Generate Busy when buffer space is low.**
- **Uniform FEM interface across the PHENIX with two different type daughter cards.**

TOF FEE diagram



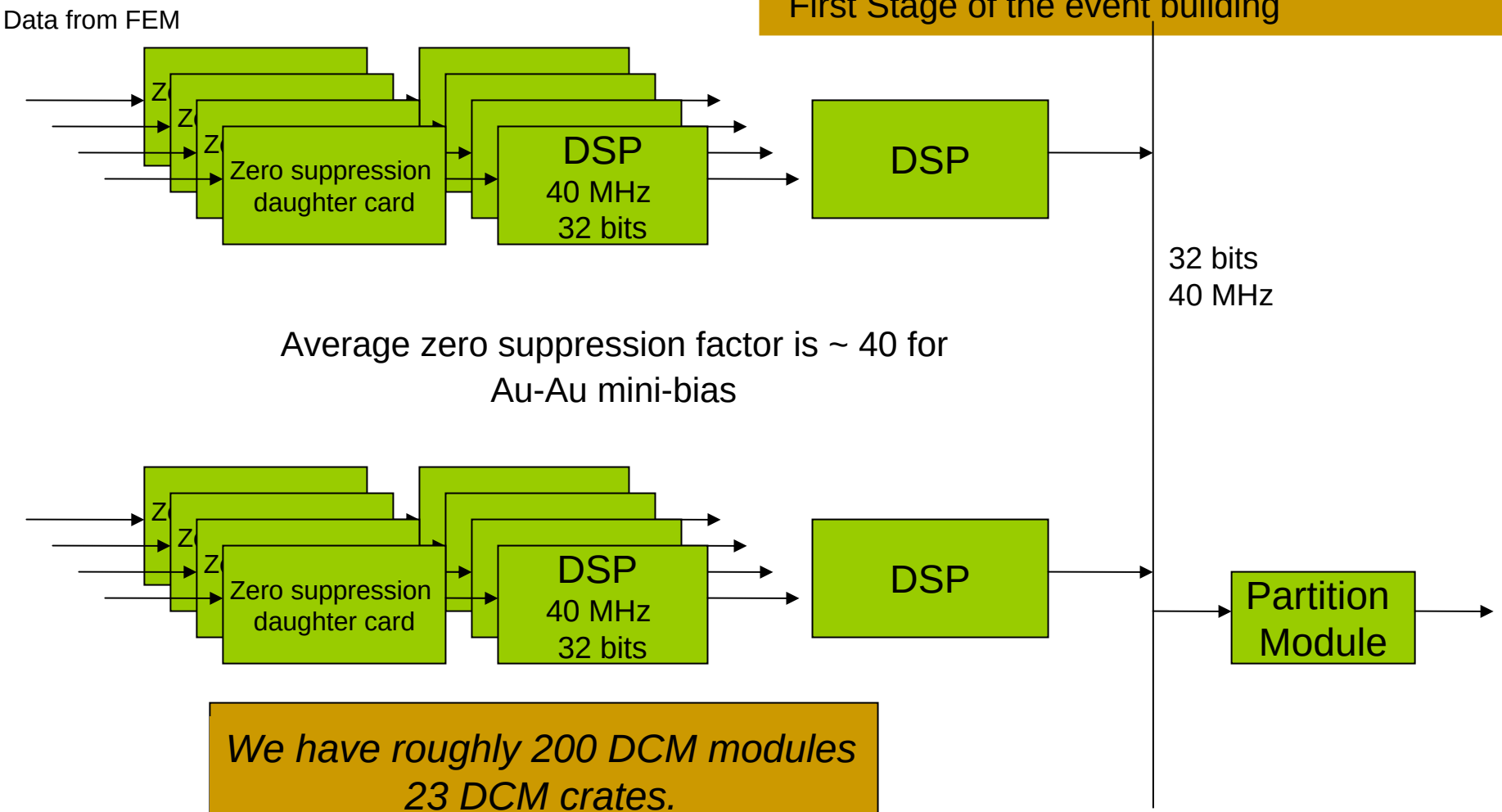
Timing System




Data Bus
Address Bus
Control Bus
VME
bus
Buffer
Local Data Bus
Scheduler
SRAM
Command
SRAM
Address Bus
Latch
Latch
Latch
To PPG
MODEBITS[23:16]
To LL1
MODEBITS[15:8]
To GLINK
MODEBITS[7:0]
Timing Subsystem
Logic
^DCMBSY[3:0]
LVL1ACCPT IN
LVL1 TRIGGER
MODE_ENABLE
ENDAT0
ENDAT1
USERBIT0
USERBIT1
USERBIT2
^GRANBSY
^COUNT5
Global
I/O
START
STOP
FIDCLK
BEAMCLK
Clock Generation
&
Phase Control
BEAMCLK
BEAMCLKX4
LVL1ACCPT
FEM

First Generation DCM

FEM can hold up to 5 L1 events
The DCM performs zero suppression,
data formatting,
multiple event buffer,
generating “BUSY”,
and error checking.
DCM has to provide 5 L1 event buffer for FEM
First Stage of the event building



We have roughly 200 DCM modules
23 DCM crates.

The simple rules

- It is a pipeline system.
- Maximum L1 trigger rate 25 KHz.
- FEM can store up to 5 L1 events.
- FEM transmits fixed format data to DCM through optical fiber.
- The DCM zero suppresses the data and provides multiple event buffers.
- DCM will raise busy if there is not enough memory.
- **System throughput can be easily calculated.**

Things we have to deal with

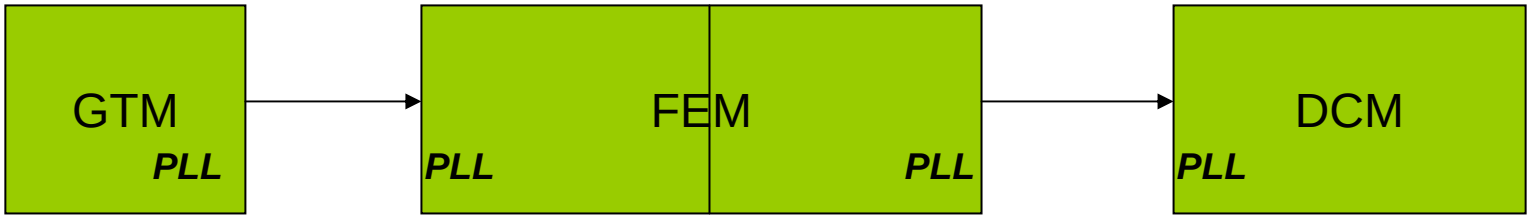
Things need to be upgraded

- Some frontend modules need to zero suppress the data before DCM
  - They need to generate busy
    - (buffer depths ??)
- We need a new DCM to deal with new detectors
  - Detectors with zero suppressed data
  - More processing demand
  - Changing technology
  - Two chips are not being produced anymore.

Things could stay the “same”

- With some modification, we can use the timing system
- The overall data volume from upgrade detectors is about 50% higher -> we can use the same event builder
- the Level 1 triggers can stay the same.

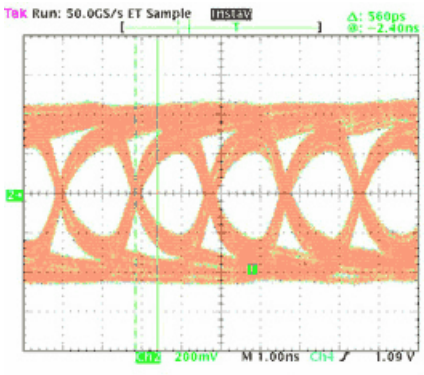
Clock jitter issues



In the current PHENIX Online system

GTM use GLINK/optical transceiver to provide FEM the clocks, L1 trigger etc.

FEM use the recovered clock to send data to DCM with GLINK+ optical transceiver.



GLINK transmitter use in coming clock to serialized data

(PLL -> average the incoming clock X24)

GLINK receiver recover the clock from the serialized data

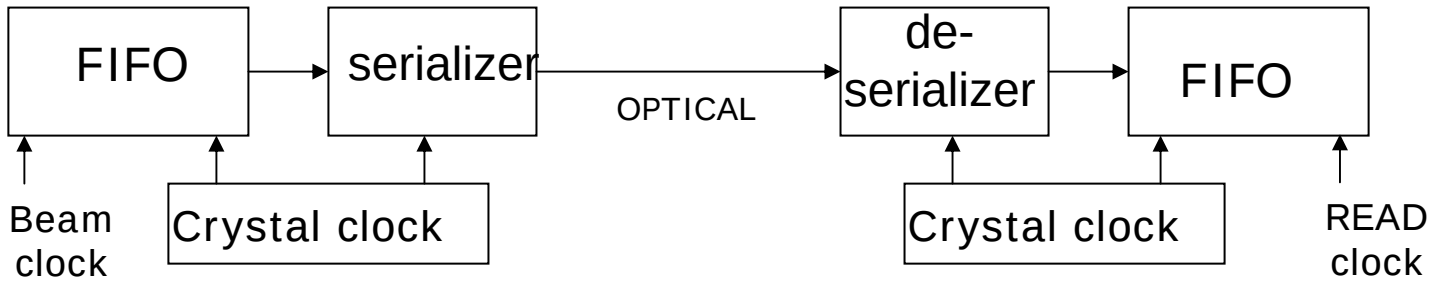
(PLL -> average of serial data frequency)

Current Data Rate 0.5/1 Gbps

Two PLL is not seeing the same variation on the clock.

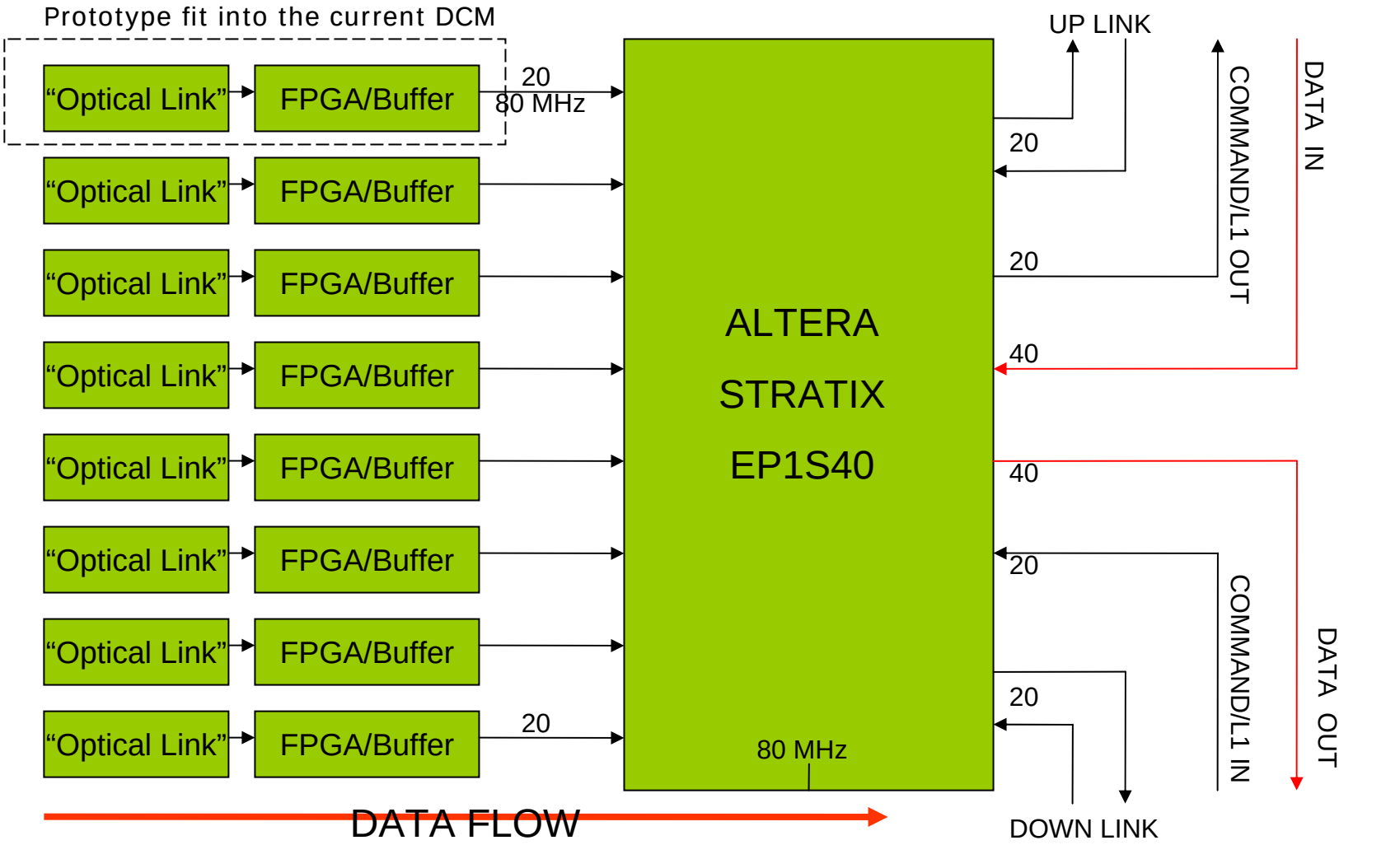
What is the issue…

- Industry want the total jitter on the clock less than 50% of the serialized data duty cycle.
  - Total jitter for 10^{-12} error rate = sigma (random jitter)*14 + data dependent jitter
- IF we use optical link at 80 MHz and 16 bits input data. The link bandwidth is 1.6Gbs with 8b/10b encoding chips.
  - The total allow jitter is only < 330ps
- This tight jitter spec may not be achievable after we transfer the clock from RHIC →GTM →FEM.
- The DCM will use crystal clock as the link clock.



NEW DCM BLOCK DIAGRAM

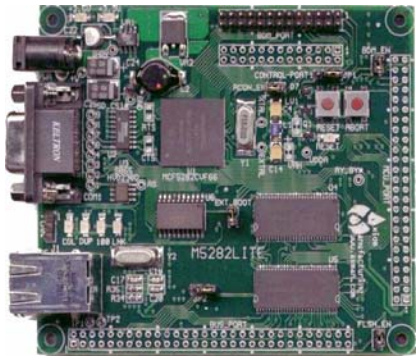
Data – formatted data output
Command – download path
Up/down link – for board/board commutations



ARCNET in PHENIX Upgrades

- Replacing ARCNET in existing FEM's is (for the most part) not practical; 350 in MUTR, 172 in EMCAL, etc. (1160 entries in node database)
- SBUS NIC's no longer made by Contemporary Control, so Sun/Solaris server will need to be replaced by…
- PCI NIC's and Linux driver (either CC supported packet driver or Jungo generated driver)
- CC PCI card based on COM20022 with DC-485 and external fiber optics

Ethernet in PHENIX Upgrades



CML-5282 Motorola Coldfire development board (3.5"x4") (www.axman.com)

- For the next generation of PHENIX FEM's, Steve Boose has been working on selecting an Ethernet based controller; same basic features as GAB, but additional capabilities possible, like an additional slow path for reading data
- Desirable features:
  - Small footprint, low profile (to fit in VME slot spacing 0.7 in)
  - Enough CPU and memory to handle ethernet traffic and control
  - Comfortable development environment
  - "Open" design so that schematics can be dropped into designs

  Some disadvantages:
  - Fatter cable; connectors probably have to be bigger RJ45
  - More software complexity
  - Point-to-point wiring and hubs necessary
- Current best idea is Freescale's Motorola Coldfire 5282 board
  - Schematic freely published; free binary monitor (RTXC)
  - Linux inside: http://www.uclinux.org/ports/coldfire/
  - About $300

PHENIX